## REMARKS

I. Status of the Application

Claims 9-28 are pending in this application. In the March 17, 2008 office action, the Examiner:

A. Rejected claims 9, 11-16, 18-21 and 23-28 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,210,828 to Bolan et al. (hereinafter "Bolan") in view of U.S. Patent No. 6,151,644 to Wu (hereinafter "Wu"), and further in view of European Patent Document EP 0599257 to Juri (hereinafter "Juri");

B. Rejected claims 10, 17 and 23 under 35 U.S.C. §103(a) as being unpatentable over Bolan, Wu, and Juri, and further in view of U.S. Patent No. 4,935,894 to Ternes (hereinafter "Ternes").

In this response, applicants respectfully traverse the rejections of the claims and request reconsideration of the application in view of the following remarks.

II. Obviousness Rejection of Claim 9

Claim 9 stands rejected as allegedly being rendered obvious over Bolan and Wu, and further in view of Juri. As will be discussed below in detail, there is no legally sufficient motivation or suggestion to combine Bolan, Wu and Juri as proposed by the Examiner. Alternatively, the proposed combination does not arrive at the claimed invention. As a consequence, it is respectfully submitted that the obviousness rejection of claim 9 should be withdrawn.

In particular, the proposed combination of Bolan, Wu and Juri does not include the following feature of claim 9:

> a control unit which is arranged to:
> ...
> store at least a first data packet of the first message in the ancillary memory *without storing the first data packet in the main memory* and store at least one other data packet of the first message in the main memory

Moreover, there is not teaching, motivation or other reason to modify the proposed combination of Bolan and Wu to incorporate the following feature of claim 9:

> wherein the main memory is of a first type, and the second memory is of a second type that is different than the first type

Accordingly, for two different reasons, it is respectfully submitted that the obviousness rejection of claim 9 is in error and should be withdrawn.

A. The Proposed Combination Does Not Arrive at the Invention

In the September 16, 2009 office action, the Examiner claimed that Bolan teaches a control unit that is arranged to "store at least a first data packet of the first message in the ancillary memory *without storing the first data packet in the main memory* and store at least one other data packet of the first message in the main memory". Applicants respectfully disagree.

In particular, the Examiner contended that Bolan teaches a control unit that receives a first message, decodes commands sent from the processors and routes them to either the processor interrupt circuitry or to mailbox circuitry, *without storing the first data packet in the main memory.* (September 16, 2009 office action at p.3). In support of the allegation that Bolan teaches bypassing the "main memory", the Examiner states that "the first data packet of

the first message is inherently passthrough the holding register (61-63 in figure 2, equivalent to the applicant's main memory...)." (*Id.*)

Thus, the Examiner has alleged that the first data packet of Bolan "passes through" the main memory (holding register 61-63) without being stored therein. Applicants respectfully disagree. Firstly, data cannot pass through a holding register 61-63 without being stored. Secondly, Bolan appears to teach specifically that all received data is stored in the holding register 61.

With regard to the first point, the holding registers 61-63 are registers. The only way that data "passes through" a register is to be stored in the register and then provided as output. Thus, the argument that data is only passthrough with regard to the registers 61-63 without being stored appears to be self-contradictory.

Moreover, even if it were *possible* to bypass storing data within a holding register and still pass the data through, it is noted that Bolan fails to *expressly* teach such functionality of the holding registers 61-63. Instead, as evidenced by the wording of the rejection, the Examiner relies on *inherency* to satisfy this claim element. It is respectfully submitted, however, that the Examiner's inherency argument with respect to this claim element is traversed. In particular, the Examiner has only alleged that it is *inherent* that Bolan teaches that a first data packet passes through the holding register without being stored. (September 16, 2008 office action at p.3). However, to show inherency, "the extrinsic evidence 'must make clear that the missing descriptive matter is *necessarily* present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain

thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (emphasis added).

In the instant case, it is *not* necessary that data *must* pass through the holding registers 61-63 of Bolan without being stored. Indeed, given that the purpose of a register is to store data, it is not only possible that the data is stored in the registers 61-63, but indeed it is very likely that the data *is* stored in the register. Accordingly, applicants respectfully disagree that the Examiner has established that the "the first data packet of the first message is *inherently* passthrough the holding register" of Bolan.

Furthermore, Bolan appears to expressly teach storage of the "first data packet" in the holding register. In particular, to the extent Bolan includes a "first data packet" as claimed, Bolan teaches that such a data packet is stored in the holding register. Specifically, Bolan states that:

> when processor 10 wants to communicate with processor 20 in the multiprocessing system, it sends information to the holding register 61. The information contains a command, an address and optionally data. When holding register 61 contains information, a request signal is passed to arbiter over request line 71, and the information is presented to the input of the multiplexor 65 on data line 74....

(Bolan at col. 4, lines 5-14). In other words, any time data is passed to the processor 20 in the Bolan system, it is sent to the holding register 61, and stays there while a request signal is sent out. Thus, Bolan clearly teaches that messages (i.e. including the "first data packet") are stored in the holding register 61.

As a consequence, for any and all of the foregoing reasons, it is respectfully submitted that the Examiner has not established that "the first data packet of the first message is inherently passthrough the holding register (61-63...)" of Bolan, and thus "without storing" the data packet in the holding register 61-63. Further, because the Examiner considers the

holding registers 61-63 to be the *main* memory, it is submitted that the Examiner has failed to establish that Bolan discloses "[storing] at least a first data packet of the first message in the ancillary memory *without* storing the first data packet in the main memory and [storing] at least one other data packet of the first message in the main memory", as recited in claim 9.

Because Bolan does not disclose a control unit arranged to "store at least a first data packet of the first message in the ancillary memory without storing the first data packet in the main memory and store at least one other data packet of the first message in the main memory", the proposed combination of Bolan, Wu and Juri does not arrive at the invention of claim 9. For at least this reason, it is respectfully submitted that the obviousness combination of claim 9 is in error and should be withdrawn.

C. No Reason to Modify the Circuit of Bolan and Wu to Include the Different Memories of Juri

Even if the proposed modification did arrive at the claimed invention, the Examiner has not provided a clearly articulated and legitimate reason for combining Bolan and Wu with the teachings of Juri.

In particular, the Examiner has admitted that the proposed combination of Bolan and Wu fails to arrive at a device that includes the limitation "wherein the main memory is of a first type, and the second memory is of a second type that is different than the first type". (September 16, 2008 office action at p.5). To address this deficiency of Bolan and Wu, the Examiner cited the teachings of Juri. The Examiner alleged that it would have been "obvious ... to modify Bolan in view of Wu to include an overflow memory as taught by Juri in order to efficiently process the data overflown from the main memory." (*Id.*)

Applicants respectfully submit that there is no reason to modify Bolan and Wu as proposed. In particular, Bolan and Wu are directed to completely different fields than that of Juri. Bolan is directed to communications between co-processors (Bolan at col. 1, lines 48-50) and Wu is directed to a buffer management system for a network packet buffer. (Wu at col. 2, lines 59-62. While these fields are at least marginally related, neither has any relationship to the technology discussed in Juri.

In contrast to Bolan and Wu, Juri is directed to a video signal recording apparatus and method. The video signal recording apparatus of Juri uses bit rate reduction suitable for devices such as VCRs. (Col. 1, lines 44-49). To this end, Juri teaches the storage of video frames on a tape. (See Fig. 1a). The data manipulation of Juri is completely unrelated to interprocessor communication (i.e. Bolan), or even network packet buffers (i.e. Wu). No one of ordinary skill in the interprocessor communication art or network buffer art would have reason to refer to Juri for any relevant teaching regarding the use of an ancillary memory.

Moreover, the Examiner has stated that the reason to include the ancillary memory of Juri in Bolan/Wu is to handle data overflows. However, Juri handles data overflows, in part, by discarding the overflow data (video frames) in the ancillary memory 8. There is nothing to indicate that it would be acceptable or applicable to discard overflow data in interprocessor communications such as those taught by Bolan.

Accordingly, it is respectfully submitted that there is no legally sufficient reason to modify Bolan/Wu with the teachings of Juri as proposed by the Examiner. For at least this additional reason, the rejection of claim 9 should be withdrawn.

C. Conclusion as to Claim 9

It is therefore submitted that the obviousness rejection of claim 9 is in error for multiple reasons. As discussed above, the proposed combination of Bolan, Wu and Juri does not arrive at the invention because contrary to the Examiner's assertion, Bolan does not disclose a control unit arranged to "store at least a first data packet of the first message in the ancillary memory without storing the first data packet in the main memory and store at least one other data packet of the first message in the main memory". In addition, there is no reason to modify Bolan and Wu to include the ancillary memory of Juri.

For at least these reasons, it is respectfully submitted that the rejection of claim 9 is in error and should be withdrawn.

IV. Claims 16, 21 and 26

Similar to claim 9, claims 16, 21 and 26 incorporate limitations identifying that the ancillary memory and the main memory are of different types. Also similar to claim 9, claims 16, 21 and 26 recite "storing at least a first data packet of the first message in the ancillary memory without storing the first data packet in the main memory, and storing one or more other data packets of the first message in the main memory", or something nearly identical thereto.

As discussed above, there is no reason to combine Bolan, Wu and Juri as proposed by the Examiner. Moreover, even if the references were combined as proposed, they would not arrive at the invention of claim 9. Accordingly, it is respectfully submitted that the rejection of claims 16, 21 and 26 over Bolan, Wu and Juri should be withdrawn.

V. Claims 10-15, 17-20, 22-25 and 27-28

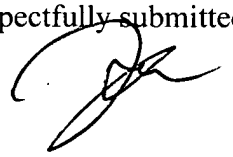
Each of claims 10-15, 17-20, 22-25 and 27-28 depends from one of claims 9, 16, 21 and 26. As discussed above, claims 9, 16, 21 and 26 are allowable over the prior art of record. Accordingly, dependent claims 10-15, 17-20, 22-25 and 27-28 are allowable for at least the same reasons.

VI. Conclusion

For all of the foregoing reasons, it is respectfully submitted the applicant has made a patentable contribution to the art. Favorable reconsideration and allowance of this application is therefore respectfully requested.

In the event applicant has inadvertently overlooked the need for an extension of time or payment of an additional fee, the applicant conditionally petitions therefore, and authorizes any fee deficiency to be charged to deposit account 13-0014.

Respectfully submitted,



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